DETAILED PROGRAM EPTC2023

DAY 1: December 5, 2023 (Tuesday)

08:00am - 1:00pm	Registration (Entrance to Grand Ballroom)	
Venue	Grand Ballroom	
08:30am - 09:00am	Opening Ceremony	
09:00am - 09:45am	**Keynote 1** Advanced System Integration Technology Trend Douglas Yu (TSMC)	
9:45am - 10:30am	**Keynote 2** Advanced Packages Enriching Heterogeneous Integration Chih Pan Hung (ASE Group)	
10:30am - 11:00am	Coffee/Tea Break (Grand Ballroom Foyer)	
11:00am - 12:30pm	**Panel Session 1 - Chiplet Integration** Moderator: Zheng Zeshan (Kaiyuan) Panelists: Ravi Mahajan (Intel), Chih Pan Hung (ASE Group), Surya Bhattacharya (A*STAR), Arvind Sundarrajan (Applied Materials)	
Venue	Grand Ballroom Foyer	
12:30pm - 1:30pm	Lunch Dining Ballroom	
Venue		
1:30pm - 2:15pm	**Keynote 3** Will Advanced Packaging Save Moore's Law? Yang Pan (Lam Research)	
2:15pm - 3:00pm	**Keynote 4** 2.5D/3D Heterogeneous Integration for Silicon Photonics Engines Radha Nagarajan (Marvell)	
3:00pm - 3:30pm	Coffee/Tea Break (Grand Ballroom Foyer)	
3:30pm - 5:00pm	**Panel Session 2 - Artificial Intelligence for Package Design and Manufacturing** Moderator: Sam Kavlakian (Emulation) Panellists: Samuel Goh (KLES), Grace O'Malley (IMEMS), Vincent Cicaporio (Applied Materials), K.N. Chiang (National Tsing Hua University), Gopal Garg (Samsung)	
6:00pm - 8:00pm	VIP Dinner (by invitation only) SAT Luncheon & Joint Ceremony	

DAY 2: December 6, 2023 (Wednesday)

08:00am - 5:00pm	Registration (Entrance to Grand Ballroom)					
Venue	Canary 1 / Canary 2		Oriole	Pelican	Kingfisher	Nightingale
08:30am - 10:15am	**PDC1** Fan-Out, Chiplet, and Heterogeneous Integration Packaging (John H Lau)		**PDC5** Automotive Electronics Reliability: Challenges and Opportunities (Pradeep Lall)	**PDC3** Co-Packaged Si Photonics: Opportunities and Challenges (Ann S. Hsing)	**PDC4** Designer-Simulation Technology for Advanced Packaging Reliability Life Prediction (K.N. Chiang)	**PDC2** Flip Chip Interconnect (Eric Perfecto)
10:15am - 10:30am	Coffee/Tea Break					
10:30am - 12:00pm	PDC1 (contd)		PDC5 (contd)	PDC3 (contd)	PDC4 (contd)	PDC2 (contd)
Venue	Grand Ballroom **EPS Luncheon** EPS Presentations; Student Travel Grant Awards Ceremony; Organizing Committee Recognition					
12:00pm - 1:30pm						
1:30pm - 2:15pm	**Technology Talk** Challenges in the Analysis and Testing of Advanced Packaging Systems Mo Shakouri (Microness LLC)					
2:15pm-3:50pm	**Sponsors' and Exhibitors' Presentations**					
3:50pm - 4:30pm	Coffee/Tea Break (Grand Ballroom Foyer)					
Venue	Canary 1	Canary 2	Oriole	Pelican	Kingfisher	Nightingale
4:10pm-6:30pm	A1. Antenna-in-Package	A2. Hybrid Bonding I	A3. Solder Materials and Processes	A4. Mechanical Simulation & Characterization I	A5. Smart Manufacturing and Equipment Technology	A6. TSV and Metallization
4:10pm - 4:30pm	**A1.1 [P101] Antenna in Package Electrical Research for Beyond 5G application** Jun. Chua Chia Liu, Sami Shih, Tony, Kang Jerome, Wang, Yu-Ruei ST-Ericsson Precision Industries Co., Ltd, Taiwan	**A2.1 [P102] High-density and high-throughput bonding technology for 3D integration** Wei-Chen Chu, Sam Shih, Tony, Kang Jerome, Wang, Yu-Ruei City University of HONG KONG, Hong Kong S.A.R. (China)	**A3.1 [P103] The trend for low temperature solder (LTS) assembly** Mukesh Ramo, Takahashi, Akarine, Tetsuya, Sasamoto, Keith Senju Superior Co., Ltd., Japan	**A4.1 [P104] The Phenomenon of Tunnel Structure Weld Floatability Experiment Result and Simulation Study** Liu, Shih Kuei, Su, Yi Hsun, Li, Zong Yuan, Chen, Tzu Chieh, Liu, Hui Chang, Lai, Ju Ming, Chen, Kuang Hsiung ARCS, Taiwan	**A5.1 [P105] Fast bending Defect Analysis using Deep Learning** Ganesh Kodali, Rahul Reddy Garapaneni, Sachin, Chandrika S.S, Rakhi B, Lavina, Prajwal Intel Net Materials, India	**A6.1 [P106] Evaluation of CZM hybrid bonding performance with SiO2/SiCN dielectric material: Interface using Finite element Model** Vijayalakshmi, Sam Kumar, Lin, Ji Chang, Sir Cheong Institute of Microelectronics, A*Star Research Entities, Singapore Singapore
4:30pm - 4:50pm	**A1.2 [P108] Characterization of POWLP Antennas in Packages** Tang Jia Jia, Lim, Teck Guan, Zhou, Lin Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore	**A2.2 [P109] Finite element simulation of Cu-SiO2 direct hybrid bonding: impact of stress bonding integration** Zhao, Guanjiang (1,2,3); Wang, Wenxin (3); Zhang, Huimin (4); Zhang, Ran (1); Zhou, Xuedong (1); Zhao, Yi (1,2,4) 1. College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China; 2. Zhejiang Lab, Hangzhou 311121, China; 3. Jiaxing University, Jiaxing 314001, China; 4. China Nanhu Academy of Electronics and Information Technology, Jiaxing 314001, China; 5. School of Electronic Information, Wuhan University, Wuhan 430072, China	**A3.2 [P110] FOWLB CS-Reversal Leadless Solder Bump Prevention** Kang Pak Meng, Kamarizan, Ha, Khai Soon, Abdul Fadzil, Muhammad Faddan NEP Semiconductors, Malaysia	**A4.2 [P111] Numerical and Experimental Investigation of Package Warpage of Large Mold Area FOWLP** Zhang, Xiaoxiao (1); Lim, Sharon P. Y. (1); Lau, Kwan Leong (1); Ren, Yong (1); Jiang, Ming Chine (1); Wang, Xiaolian (2); Liu, Sengfei (2) 1. Institute for Infocomm Research (I2R), A*STAR, Singapore; 2. Institute of Materials Research and Engineering, A*STAR, Singapore	**A5.2 [P112] Efficient and Adaptive Semantic Segmentation of HRMs using Incremental Learning** Zhang, Richard (1); Wang, Jim (1); Thakur, Kamala (1); V. Nair (1); Cheng, Ser Choon (2); Pattan, Ramanpreet Singh (1) 1. Institute for Infocomm Research (I2R), A*STAR; 2. Institute of Microelectronics (IME), A*STAR	**A6.2 [P113] Defect evolution during through silicon via copper electroplating and methods for robust void-free filling** Tan, Van Nhat Anh; Venkatarraman, Nandini; Tan, Wang Tong; Ye Ching Wang; Kangan, Chai; K. L Singh; Nandy Srinivasa Rao, Vincent Agency for Science, Technology, and Research - Institute of Microelectronics, Singapore
4:50pm - 5:10pm	**A1.3 [P114] 3-band LTC Phased Array AiP for Automotive Applications** Abdelhalim, Ahmed Shehata (1); Zhai, Xiaoyun (1); Pietikainen, Mari Kristiina (1); Manuel, David Ryan (1); Kaunisto, Mikko (1); Huang, Guoliang (2); Pinel, Sergio (1) 1. Huawei Technologies, Canada; 2. Huawei Technologies, Chengdu Base	**A2.3 [P117] Grain boundary analysis of Cu-Cu hybrid bonding using ACOM-TEM** Fujiwara, Ryosuke; Yasuda, Mitsunobu; Tanaka, Nobuaki; Shimada, Yuki; Kawasaki, Naofumi; Otsuka, Yuji Toray Research Center, Inc., Japan	**A3.3 [P118] Modifying of solder composition on ENIG for high TC reliability on Cu-OSP** Sun, Jae Yeol (1,2); Lee, S.D (1); Lee, Y.W (2); Jung, S.B (1) 1. MEA Korea, Republic of (South Korea); 2. Sungkyunkwan university, Korea, Republic of (South Korea)	**A4.3 [P119] Identify critical packaging parameters impacting wafer warpage using FEA and statistical analysis** Ji, Lim Ng; Ng Teng Chyn Institute of Microelectronics Singapore, Singapore	**A5.3 [P120] Study on Enhancing Flip Chip Die Sorter Package (FCDS) Reliability Testing using Deep Learning-Assisted SAM** Sakunwarachart, Nan; Jiaj, Qi; Kiyoto Wooram; Ong, Ai Ling; Ng, Kok Ann; Ong, Ai Ling; Ong, Chong; Kamesu, Feng; Kuo Kang Ming Kaohsiung (1); Wei, Regan (1); Kamesu, Zun (1); Wang, Rachel (1); Cascade, Peter (1); Hu, Kevin (1); Kao, Chun Chang (2); Ku, Chun Fu (2); Yen, Jacter (2)	**A6.3 [P121] Wafer level fabrication of Embedded Silicon Microchannel on Heating Devices** Lee, Beom Joong; Ong, Jacter; Jin, Jeoen; Jeong Ki Ong; Zheng, Xiamen; Feng, Kuo Kang IME Jacter, Singapore
5:10pm - 5:30pm	**A1.4 [P116] Design of 27GHz band Gamma on chip and wire-bonded antennas** Kim, Ryoung; Ryu, Taehyoung; Kanya, Kazuichi Kyoto University, Japan	**A2.4 [P124] RC delay mitigation for sub 750nm Hybrid bonding pitch** Uhnels, Sandriesser (1); Ayoub, Bacvar (1,2); Fromsel, Helene (1); Morrow, Stephanie (1); Marmus, Sebastian (1); Gabdhe, Sneha (1); Gaudron, Emeline (1); Guerrini Carlos, Maria Catarina (1); Isabelle, Fox (1); Lamontagne, Bruno (1); Ray, Christelle (1); Tournier, Arnaud (1) 1. STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France; 2. IMT-Atlantique, Technopole Brest-Iroise CS 83818 29238 LUCE, CEDEX Technopole Brest-Iroise, Grenoble Alpes, CEA, LETI, 38000 Grenoble, France	**A3.4 [P117] Indium based Flip-chip interconnect for Cryogenic Packaging** Jaeger, Berthold; Hoegen, Lu Ser Chuang; Chang, Kai Chu Institute Of Microelectronics, Singapore	**A4.4 [P125] Impact of Wafer Pre-chip Thickness on Stud-Bump Performance** Sun, Dae Sun (1); Yampatu, Venkata Rama Satya Pradeep (1); Kim, Mina Kwan (1); Singh, Kanjalochan Vem (1) 1. Micron Semiconductor Asia Operations Pte. Ltd. (MSAO), Assembly Technology Development, India; 2. Micron Memory Taiwan Co. Ltd., Taiwan	**A5.4 [P123] Anomaly Detection for Dispensing of Solder Paste on SD Small Carriers Using Machine Learning** Tiesler, Nils; Wagner, Marcus; Meier, Sven; Kogel, Christian; Franke, Jörg Friedrich-Alexander-Universität Erlangen-Nürnberg, Institute for Factory Automation and Production Systems, Germany	
6:00pm - 9:00pm	Banquet Dinner					

DAY 3: December 7, 2023 (Thursday)

Venue	Canary 1	Canary 2	Oriole	Pelican	Kingfisher	Nightingale
08:30am -09:00am	**Invited Talk 1** 3D Integrated Package for High Performance Computing Applications (YinPo Wang, SPIL)	**Invited Talk 2** Wafer-to-Wafer and Die-to-Wafer Hybrid Bonding for Advanced Interconnects (V. Dragoi EVG)	**Invited Talk 3** Development Novel Polymer Materials for Advanced Packaging (Takenori Fujiwara, Toray)	**Invited Talk 4** The Era of Generative AI and Advanced Packaging (Chak Wing Kok, ASMPT)	**Invited Talk 5** AI and Failure-Mechanics-Based Life Prediction for Electronic Packaging (Pradeep Lall, Auburn Univ.)	**Invited Talk 6** Forward-Looking Roadmap View to Enable Heterogeneous Integration Technology Trends (Eamon Hynes -Khrone, AMD)
09:00am -10:00am	B1. Interconnects in Advanced Packaging	B2. Hybrid Bonding II	B3. Materials and Processing I	B4. Mechanical Simulation & Characterization II	B5. Solder Reliability	B6. Cooling Solutions for SiC
09:00am - 09:20am	**B1.1 [P131] Challenges of Scaling Down High Power Performance Flip Chip Ball Grid Array (FCBGA) Package** Chuan, Wang Hoong; Lakhera, Kishorey; Ladhing, Trent; Bhavathkar, Jagannath; Ravindranath, Sandeep; Mohd Salleh, Juhaini INEM Semiconductor, Malaysia	**B2.1 [P132] UHD (Laser Assisted Bond) bonding evaluation** Kim, Gyihyun Amkor Technology Korea, Korea, Republic of (South Korea)	**B3.1 [P133] Development of micron-sized sp3 C-composite paste die attach material** Chen, Zhuoxiang (1); Liu, Yang (1); Wanagun (1); Inshima, Mitsuru (2); Nakayama, Koji (1); Suganuma, Katsuaki (1) 1. Osaka university, Japan; 2. Daicel Corporation	**B4.1 [P134] Mechanical Modelling and Analysis of CMOS Image Sensor Package** Lim, Teck Kiang (1); Sukimon, Muhammad Ridzuan (1); Bur Kiran, Sawan Manoharrao (1); Subhash, Jasmine (1) 1. ON Semiconductor (M) Sdn Bhd; 2. Universiti Teknikal Malaysia Melaka (UTeM)	**B5.1 [P135] Recipe Tin Lead-Free Solder Paste for Advanced Packaging** Sudrun Long, Wen Sang Peng, Hui Bryant, Jia, Ken Ting; Jason Lim, Chan Mitz Tan, Tan Ding Sing, Tong Kyat Yoneda Materials Singapore Pte Ltd., Singapore	**B6.1 [P136] Transient thermal characterization and analysis for next generation HC power module** Tang, Dong Yun; Ye, Hong Liang; Wei, Jiong Ching; Pan, Yang Institute of Microelectronics, Singapore
09:20am - 09:40am	**B1.2 [P139] Thermo-Mechanical performance of large body and small pitch flip chip packaging using higher layer count substrates with BGRW solder pad finish** Ramasamy, Jeevandar (1); Singh, Inder(1,2); Ng, Jon (1); Mahoney, Gerry (1); Low, Kim (1); Kim, Dae (1) 1. UMS, Singapore; 2. UMS, San Jose; 3. UMS, Singapore; 4. UMS, San Jose; 5. UMS, San Jose; 6. UMS, San Jose	**B2.2 [P140] Characterization of Hybrid Bonding through using Atomic Force Microscopy** Shin, Dongguy; Moon, Bumki; Jae, Yongho; Woo, Sinwoong; Lee, Byungjoon; Khim, Minsoo Samsung Electronics	**B3.2 [P141] Characterization of Differential TSV Vertical Interconnects in 500MHz with Double Side Measurement** Wu, Fang (1); Lim, Teck Guan (1); Liew, Jason; Tsung Fang (2); Guo Boshu, Sejay Bhuvanendran Nair (1) 1. Institute of Microelectronics, A*STAR, Singapore; 2. Nan Tree Photonics Pte Ltd, Singapore	**B4.2 [P142] Reliability prediction and improvement of board level thermal cycling test for enabled FC BGA array** Chen, Kai Hong (1); Chen, Yung Kuan (1); Lai, Alex Wei (1); Kao, Chun Hung (1); Hu, Wei Ge (1); Kao, Chun Hung (1); Hu, Chun Yu (1); Cheng, Chi Min (2) 1. Product Characterization, Advanced Semiconductor Engineering, Inc., Taiwan; 2. Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, Taiwan	**B5.2 [P143] Excellent Reliability Organic Thermal Interface Materials for SC Power Module** Nakamura, Sotaroo (1); Sakaba, Yohei (1); Shimada, Akira (2) 1. Toray Singapore Research Center; 2. Toray Industries, Inc.
09:40am - 10:00am	**B1.3 [P144] Back Side Metallization for Logic Application** Sebastiaan, Reinard (1); Dalenbrier, Ralph (1); Lim, Stanley (1); Singapore, Sunish Kumar (1); Tarsan Branch, S Branch 9B.Pte Ltd		**B3.3 [P145] Investigations of Two-Stage Ag Sintering Processes for the Die Attach of Power Devices** Sunkelder, Dennis (1); Wachsmann, Marco (1); Kähler, Martin (1); Lewinsky, Marvin (1); Wierzbicki, Johannes (1); Bauernfeind, Curt Georg (1); Meuch, Nicolas (1) 1. Hanns-Lippisch-University of Applied Sciences, Germany; 2. Sentinor Gerlach, Nuremberg, Germany	**B4.3 [P146] Micro Profile related Design for Reliability for Power Electronics based on Finite Element Simulation** Mikowski, Jan (1,2); Mers, Tobias (1); Gabrielsson, Sandra (1); Bergfors, Sven (1,2) 1. Fraunhofer IISB1, Technologiezentrum 3, Erlangen, Germany; 2. Friedrich-Alexander University Erlangen-Nürnberg, Center for Microelectronics, Betriebsstätte Staedtler 70, 90518 Cadolzburg, Germany; 3. Siegmund-Schuckmann-Str 16D, 22529, Hamburg, Germany	**B5.3 [P147] Sandwich Reliability Organic Thermal Interface Materials for SC Power Module** Nakamura, Sotaroo; (1); Sakaba, Yohei (1); Shimada, Akira (2) 1. Toray Singapore Research Center; 2. Toray Industries, Inc.
10:00am - 10:30am	Coffee/Tea Break (Grand Ballroom Foyer)					
Venue	Canary 1	Canary 2	Oriole	Pelican	Kingfisher	Nightingale
10:30am - 11:50am	C1. Hybrid Bonding in Advanced Packaging	C2. Wirebonding Processes	C3. Bonding Materials and Processes	C4. Mechanical Simulation & Characterization III	C5. Reliability I	C6. Thermal Management I
10:30am - 10:50am	**C1.1 [P148] Edge Detection Algorithm for Thermal Alignment Marks in Hybrid Bonding** Sugiura, Takamasa (1); Nagatomo, Daisuke (1); Kajiyama, Masaaki (1); Akazawa, Shinji (1); Tokunaga, Takafumi (2); Qin, Seungjoon (2); Kim, Sungwon (2); Chen, Xuexue (2); Wan, Shaoang (2); Ian, Hoyoin (2); Jae, Byungjoon (2); Khim, Minsoo Samsung (2) 1. Samsung Japan Corporation, Samsung Device Solutions R&D Japan; 2. Samsung Electronics Co., Ltd, Metrahomics Research	**C2.1 [P151] Characterization and Reliability of Al and Al-coated Cu Wires for High Power Applications** Fouzia, Ramakrishnan Nair (1); Fuchs, Hans Jurgen (2); Bolsdorf, Sven (2); Hellwich, Ulrich (2); Lugauer, Christian (2); Tai, Hong Mun (3); Pan, Hailao (3); Yao, Pei Lian (3); Chua, Kai Ren (3) 1. Beyond-a-Hong Kong, Hong Kong S.A.R.; 2. Beyond-a-Germany GmbH; 3. The Hong Kong University of Science and Technology, Hong Kong S.A.R.; 4. Guangzhou Institute of Science and Technology (Guangzhou), Guangzhou, P.R. China	**C3.1 [P152] Exploring Bond Strength for Advanced Chiplet with Hybrid Bonding** Tuan, Junya; Iwata, Tomoyo; Yoichiura, Ken; Kuno, Marie; Inoue, Yuichiro(1) Yokohama national university, Japan	**C4.1 [P153] Design Optimization to Boost Solder Joint Reliability Performance for 100 BGA Package** Lee, Ing (1); Lee, Yik Fai Ring (1); Lee, Wei (1); Lee, Jason chen (1); Ng, Hongwei (1); Tan, Kelvin Sin Boo (1); Tam, Wan wai (1); Kohle, Alexander (2); chen, ing-wei (3) 1. Micron Semiconductor Asia Operations Pte. Ltd. 2. Micron Technology, Inc., 3. Micron Memory Taiwan Co	**C5.1 [P154] Improving Board Level Reliability of a MEMS Heat Sink, Big Bga Microbumb with Sidewall Bite** Alexander, Farell (1,2); Alexander, Saeed (1,2); Mathew, Bobby (1,2) 1. United Arab Emirates University, Mech. Engineering, Al Ain, United Arab Emirates; 2. United Arab Emirates University, National Water and Energy Center, United Arab Emirates	**C6.1 [P155] Thermohydraulic Characteristics of a MEMS Heat Sink, Big Bga Microbumb with Sidewall Bite** Alexander, Farell (1,2); Alexander, Saeed (1,2); Mathew, Bobby (1,2) 1. United Arab Emirates University, Mech. Engineering, Al Ain, United Arab Emirates; 2. United Arab Emirates University, National Water and Energy Center, United Arab Emirates
10:50am - 11:10am	**C1.2 [P156] Alignment Vision System for Hybrid Bonding in Advanced Packaging** Nagatomo, Daisuke (1); Sugiura, Takamasa (1); Kajiyama, Masaaki (1); Akazawa, Shinji (1); Tokunaga, Takafumi (2); Qin, Seungjoon (2); Kim, Sungwon (2); Chen, Xuexue (2); Wang, Shaoang (2); Ian, Hoyoin (2); Jae, Byungjoon (2); Khim, Minsoo (2) 1. Samsung Japan Corporation, Samsung Device Solutions R&D Japan; 2. Samsung Electronics Co., Ltd, Metrahomics Research	**C2.2 [P157] Characterization and Reliability of Pd and Pd-coated Cu Wires for High Power Applications** Fouzia, Ramakrishnan Nair (1); Fuchs, Hans Jurgen (2); Bolsdorf, Sven (2); Hellwich, Ulrich (2); Lugauer, Christian (2); Tai, Hong Mun (3); Pan, Hailao (3); Yao, Pei Lian (3); Chua, Kai Ren (3) 1. Beyond-a-Hong Kong, Hong Kong S.A.R.; 2. Beyond-a-Germany GmbH; 3. The Hong Kong University of Science and Technology, Hong Kong S.A.R.; 4. Guangzhou Institute of Science and Technology (Guangzhou), Guangzhou, P.R. China	**C3.2 [P158] Novel Solder Wire Selection Methodology for High Reliability Automotive IC packages** Fontes, Raquel Jacoana; Renard, Jairo; Oliveira, Leandro; Sá, Bruno; Silva, Gilberto (1); Apagaer Gangamalli, Rama (1); Kunz, A Mahdi (1) 1. Applied Materials, United States of America; 2. Applied Materials, Singapore	**C4.2 [P159] Investigation on Underfill Properties Effect on Board Level Solder Joint Reliability for BP Package** Pan, Fanying (1); Ong, Yewe Chen (1); Pyn, Jing (1); Yu, wei (1); Ng, Hongwei (1); Chen, Wilter (2) 1. Micron Semiconductor Asia Operations Pte Ltd, Singapore; 2. Micron Memory Taiwan Co	**C5.2 [P160] ACCEPTANCE CRITERIA FOR SOCO-SOLDER JOINT RELIABILITY ON WAFER LEVEL CHIP SCALE PACKAGE (WLCSP) AT LARGE DIMENSIONS** Ramasamy, Sukeshini; Supramaniam, Sarasvathy; Abdullah, Mohammad Nishfikhan; Balasubramanian, Selvakumar Kaspersky, Malaysia	**C6.2 [P161] Experimental Investigations on the chip thermal coupling effect by embedded-manifold cooling** Ye, Yuan'o; Kang, Yanmei; Du, Xiangkun; Liu, Ruiyao; yan, Shizhong; Ji, Ailan; Xiao, Bowei The Institute of Microelectronics of the Chinese Academy of Sciences, China, People's Republic of
11:10am - 11:30am	**C1.3 [P162] Reliability Assessment of 2.5D Module using Chip to Wafer Hybrid Bonding** Chang, Jen Chang; Jamon Ou, Kang Sung; Chen, Chia Chen; Chen, Ming Ji; Chen, Chien Chung; Sunali, Mishra; Jitinder, Mishra; Sriram, Rao Institute of Microelectronics, Singapore	**C2.3 [P163] Insulated, Passivated & Adhesively Protected Bond Wire using ACOS Coating** Park, Sangwell OnWires Co., Ltd., Korea, Republic of (South Korea)	**C3.3 [P164] Polymer Dielectric Materials Evaluation for Hybrid Bonding Applications** Tsuzuki, Ragnarella Sofiner (1); Tsuzuki, Ragnarella Sofiner (1); Tsuzuki, Ragnarella Sofiner (1); Ribeiro, Jose (1); Oliveira, Jose (1); Kelly, Norman (1); Mitchell, Gilmay Kumar (1); Chang, Jen Chang (1); Sampat, Srinivasa Rao (1) 1. Institute of Microelectronics, A*STAR, Singapore; 2. Toray Industries, Inc. Japan	**C4.3 [P165] Copper/Matching Compound Interfacial Determination** Pandey, Mayank (1); Jarrett, Samuel (1); Ramos, Ricardo (1); Ribeiro, Jose (1); Oliveira, Jose (1); Kelly, Norman (1); Mitchell, Gilmay Kumar (1); Chang, Jen Chang (1); Sampat, Srinivasa Rao (1) 1. Institute of Microelectronics, A*STAR, Singapore; 2. Toray Industries, Inc. Japan	**C5.3 [P166] Impact of Underfill Material Network and Filler Element Simulation for Package Warpage Prediction** Gangopaty, Sunil Kumar (1); Zhao, Fu Jing (1); Ang, Yeow Chon (1); Bauer, Pascual Bugenhagen (1); Ng, Hong Wan (2) 1. Micron Technology Operations India LLP, India; 2. Micron Semiconductor Asia Operations Pte Ltd. 990, Bendemeer Road, Singapore
11:30am - 11:50am	**C1.4 [P167] Optimization of CMP process for direct wafer to wafer oxide bonding** Sivagnanam, Chandrasekaran; Hemanth Kumar, CH; Ting Sie, Lilli; Hui Ang, TMD; Wei Ho, BBG; Sung Kun, Li; Hong Yu, CHRN; Sven Gaus; Venkatraman, Nandini; Lilli, Wenli Institute of Microelectronics (IME), A*STAR, Singapore	**C2.4 [P168] Moisture- and Solder Induced Degradation of Silver Wire and Silver (Aluminum Based Ribbon)** Grafenberg, Sam Harvey; Ko, Jonathan STMicroelectronics, Inc., Philippines	**C3.4 [P169] Aged-aged Optical Detection of Chipping Defects in a Die Sorter** Aubert, Norbert; Mirabelon, Andreas; Zang, Guodong; Farnagiel'ar, Farnaz Besi Switzerland AG, Hinterbergstrasse 32a, 6330 Steinhausen, Switzerland	**C4.4 [P170] Effect of Underfill on Substrate Tense Deformation PIC** Yu, Wei (1); Pyn, Jing (1); Tan, Kelvin (1); Chu, Fu Ring (1); Ong, Yewe Chen (1); Ng, Hong Wan (1); Fan, Richard (2) 1. Micron Semiconductor Asia Operations, Singapore; 2. Micron Memory Taiwan Co., Ltd., Taichung city, Taiwan	**C5.4 [P171] Repaction based warpage delamination detection method for integrated fanout package in strip form** Zou, Tai (1); Khaw, Lee Lin (1); Tan, Joseph (1); Lee, Jerry (1) 1. Amkor Technology Singapore, Singapore; 2. STMicroelectronics Singapore; 3. STMicroelectronics
Venue	Grand Ballroom **EPTC Luncheon** EPTC Highlights; Sponsorship; Exhibition Appreciation Ceremony					
12:00pm - 1:30pm						
1:30pm-3:00pm	**Sponsors' and Exhibitors' Presentations**					
Venue	Canary 1	Canary 2	Oriole	Pelican	Kingfisher	Nightingale
1:30pm-3:00pm				**Region 10 Chapter Chairs' Meeting**		
Venue	Canary 1	Canary 2	Oriole	Pelican	Kingfisher	Nightingale
3:00pm - 6:00pm	D1. 2.5D/3D Packaging Technologies	D2. Bumping Technologies I	D3. Materials and Processing II	D4. Mechanical Simulation & Characterization IV	D5. Emerging Technologies	D6. Advanced Optoelectronics and Displays I
3:00pm - 3:20pm	**D1.1 [P180] Packaging strategies for Photonic and Electronic chips on a Glass substrate** Barmen, Robert (1); Wickert, Karl (1); Gupta, Pernika (1); Bonna, Luigi (1); Wenninger, Drew (1); Agarwal, Jaswantha (2); Tamar, Samuel (3); Ramos, Ricardo (3); Ribeiro, Jose (3); Greenberg, Lionel (3); O'Brien, Peter (3) 1. Tyndall National Institute, University College Cork, Ireland; 2. Massachusetts Institute of Technology, Cambridge, MA; 3. Bridgewater State University, Bridgewater, MA, USA	**D2.1 [P181] Low temperature solder for low surface-wetting process** Wang, Yi Shan; Liang, Hua Tai; Tung, Tao Ping; Wu, Sian Shuei Tamkang University, Taiwan	**D3.1 [P182] Warpage Behavior of Different Fan-out Chip First Wafers** Zarnhe, Debbie Claire IBS, Germany	**D4.1 [P183] Hard bond pad plastic deformation and contact resistance simulation for SOT-MRAM modeling of wire-bonding process** guerrini, lorenzo; caglio, carlotta; villa, riccardo; zaner, beatrice; passaglia, carlo; cascella, luca(1) CNR-nanotechnology, Italy	**D5.1 [P184] Flexible ICs Developed by Electrochemical Deposition of Metal Oxides Sensors for CMOS Image Sensors** Goto, Masahiko; Iwata, Shigeyuki; Sato, Kiyoaki NHK Science & Technology Research Laboratories, Japan	**D6.1 [P185] Solutions for Process Challenges in Fabrication of Microchannels for Microfluidic Photonic Integration** Chia, Lai Yee; Bhuvaneswari Nair Gopi Sudhy; Sejay, Ho; Sean Wolf Institute of Microelectronics, A*STAR, Singapore
3:20pm - 3:40pm	**D1.2 [P186] Bridge Die Compensation & Adaption Patterning in a Multi Die Module in HDI mm Format** Sandstrom, Clifford (1); Tulsie, Erick (1); Sale, Ken Kenneth (1); Fang, Jem Kuang (1); Yang, Ping Fang (1); Huang, Sheng Ping (1); Shen, Ping Hong (1) 1. Aleo Technologies, United States of America; 2. ASE Technology, Taiwan	**D2.2 [P187] Investigation of Using Superconductivity on Solder Material for Cryogenic Packaging** Ng, Teng Chyn (1); Li, Hongxia (1); Binte Abdul Rashid, Nur (1); Soh, Kuan Eng Johnson (2,3,4); Huang, Ding (3); Lau, Chit Siong (3); Ong, Ai Ling (3); Chen, Chinna Gong (3); Chai, Ang Ai (3) 1. Institute of Microelectronics (IME), Agency for Science Technology and Research - (A*STAR); 2. Institute of Materials Research and Engineering (IMRE), Agency for Science Technology and Research (A*STAR); 3. Department of Physics, National University of Singapore (NUS); 4. Division of Physics and Applied Physics, School of Physical and Mathematical Sciences, Nanyang Technological University (NTU)	**D3.2 [P188] A Novel Approach to Enhance the High Reliability of Solder Joints through Intermetallic Reliability Prevention of Solder Interconnect** Su, Hsuan-Ping; Hsu, Ming-Hsuo; Chen, Chih Hsiang; Huang, Augustt Siliconware Precision Industries Co., Ltd., Taiwan	**D4.2 [P189] Study on Using Noisy Synthetic Data for Neural Networks to Assess Thermo-Mechanical Reliability Parameters of Solder Interconnects** Mikowski, Oliver; Hübner, Robert (1); Bartus, Chanchan; Meier, Karsten; Bach, Ken Bernd (2) Technische Universität Dresden, Institute of Electronics Packaging Technology, Dresden, Germany	**D5.2 [P190] Process Development and Integration on Si Substrate for Ion trap-based Quantum Processors** Ai, Hongqiu (1); Liu, Clarence Ho Hoching (2); Hello, Nathan Bernard; Sachet (1); Jimenez, Christian; Ahmad (1); Mohrs, Silvana (1); Ramirez, Jorge (1); Ramirez, Jorge (1); Wolfenstyne, Marcus (1,4); Chou, Ang Lee (1,3) 1. IME, Singapore; 2. CQT/NUS, Singapore; 3. AMD, Singapore	**D6.2 [P191] Design and Fabrication of a Test Board assembly for a Silicon Photonics LiDAR Device** Sieve, Mark (1); Frisende, Antonio (1); Maggi, Luca (1); Sabbione, Daniele (1); Cancellieri, Filippo (1); Radke, Daniel (2); Gerstner, Thomas (2); Ortsiefer, Markus (2); Ortsiefer, Markus (2

4:20pm - 6:00pm	**O1.1 (P1.17) 2.5-D MODELING OF FAN-OUT PANEL LEVEL PACKAGE (WO-FO WAFERLEVEL SUPPERSEDED SOLUTION)** Singh, Shivendra Pratap; Pancharia, Vishwanath Pandurkhe; Lu, Zheng Yuan National Tsing Hua University, Taiwan	**O1.2 (P1.18) Polymer-Based Dual Damascene Process for Fine Pitch RDL Advanced Packaging** Hsiao, Hsi-ping; Tan [1]; Jay; Ryan [2]; Sun; Peng [1]; Yang; Andy; Chang; Kuo [1] 1. Institute of Microelectronics / Agency for Science, Technology and Research, Singapore; 2. Packaging Process Integrations, Advanced Packaging Development Center, Applied Materials, Inc.	**O1.3 (P1.19) Development of Thin 3-D-SiGe/Si Film Fabrication on Transparent wafer in 200mm CMOS fab** Vos, Tom; Van Dieten, Bert; Tack, Klaas; Vasseur, Denis; Bulcaen, Hugo imec, Belgium	**O1.4 (P1.20) Thin 3' Chip Fabrap Process Risk Analysis and Experiments in conjunction with Advanced Approach** Tsai, Y. Hsuan [1]; Shankaran; Sandeep [2]; Lu; Yen Chi [1]; Fang; Yao Jung [1] 1. NXP Semiconductors, Taiwan; 2. NXP Semiconductors, TX, USA	**O1.5 (P1.21) Electromigration Study of Cu Filler Interconnects in FC QFN Packaging Under High Power Devices** Tsai, Min Hsin [1]; Kao, Chin Li [1]; Wang, Yuan Ru [1]; Lu; Yung Sheng [1]; Liang, Chien Long [2] 1. Advanced Semiconductor Engineering, Taiwan; 2. National Taiwan University of Science and Technology, Taiwan	**O1.1 (P1.22) Artificial Intelligence aided design for heterogeneous integration system in package** Huang, Lulu [1]; Zhao, Jiajing [1]; Gao; Jiajing [1]; Jiang, Huaxia [1]; Li, Jianfeng [1] 1. Huawei Technologies Co., Ltd, China, People's Republic of; 2. Huawei Device Co., Ltd, China, People's Republic of	Interactive Presentations 2
4:40pm - 6:00pm	**O1.6 (P1.91) Development of Large 400 Hexapanel Package using 55L-Fine FOWLP Process** Ho, Soon Wee Gerald; Soh, Siew Boon; Lee; Boon Long; Hsiao, Hsi-ping; Rao, Vempati Venkanna [1,2] Institute of Microelectronics, A*STAR, Singapore	**O1.7 (P1.92) Improvement in Wafer-to-Wafer Hybrid Bonding using Optimized Thermal Mechanical Planarization process for Cu Dishing** Khanna, Gaurav [1]; Pancharela, Sulkarna [1,2] 1. Institute of Electronic Packaging Technology, Technische Universität Dresden, Dresden, Germany; 2. JCET-STATS ChipPAC Korea Limited, Seongnam, Korea, Republic of; Fraunhofer Institute for Reliability and Microintegration (IZM), Dresden, Germany	**O1.8 (P1.93) Development of Thin 3-D-SiGe/Si Film Fabrication Application** Sharma, Jatin; Chen; Daniel Xiao; Tan; Teng Shun; Ho Institute of Microelectronics, Singapore	**O1.9 (P1.94) Capillary Underfill Flow Simulation and Experimental Study for Solder Mask Opening and Trace Distribution** Lee, Jin Hsien [1]; Yang; Shin Yueh [1]; Liu, Kahan [1]; Chen; Bongsoon [1]; Chia; Yonte Chen [2]; Ng; Kiang Wee [2] 1. Siliconware Memory Taiwan, Co., Ltd.; 2. Siliconware Memory Taiwan, Co., Ltd.; 3. Siliconware Memory Taiwan, Co., Ltd.; 4. Siliconware Semiconductor Asia Operations Pte Ltd.; 5. Siliconware Semiconductor Asia Operations Pte Ltd.; 6. Siliconware Semiconductor Asia Operations Pte Ltd.	**O1.10 (P1.95) Detection of bending cracks in multi-tier stacks with SAM** Chen, Gang [1]; Gaikwadwani; John [1]; Raghavendra; Jamuna [1]; Bhavana; Shetty [1]; Zhang; Bruce [1]; Schlatcher; Fritz [1]; Auffrappe; Peter [2]; Schaefer; Ingo [2]; Phomkeuthong; Alain [2]; Benet; Christopher [2]; Ho; Chee Hong [3]; Ong; Ai Ling [3]; Chan; Kim Leon [3]; Leong; Philip Lyn [3] 1. ASMC, Belgium; 2. PVA TePla Analytical Systems GmbH, Deutschweinebraten 58, 79283 Bollenhausen, Germany	**O1.11 (P1.96) A NOVEL STRUCTURE OF MULTI-BEAM INTERFEROMETER WITH LINE LOSS** Li, Zhenyu [1]; Li; Shan [2]; Lai; Wei [3]; Ma; Ming [1]; Wen; Jian [1] 1. S&A, A-STAR, SINGAPORE, Singapore 2-438, SES, SINGAPORE	
5:00pm - 6:20pm	**O1.12 (P1.14) Method of Triple Thin Film IDU Layers on a 200 Substrate** Chen; Yi-Hao [1]; Ho; Yip Chung [1]; Lee; Jeffrey Chengfeng [2] 1. PiTec Co., Ltd., Taiwan; 2. ST Integrated Service Technology Inc., Taiwan	**O1.13 (P1.15) Evaluation of Low Temperature Inorganic/Dielectric Materials for Hybrid Bonding Applications** Mishra, Dhiraj Kumar; Gourav; Aggarwal; Sekhar; Chang; Ser Chiang; Bhowmik; Chandan Rao; Chen, Ang Jen; Wenqian; Srinivasa Rao[1] Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore	**O1.2 (P1.16) Experimental Study on Thermal Stress Induced Warpage Of Fan-Out Wafer Level Packaging** Wang, Pei-Wei; Lin, Tai Wei; Dai, Jeng Gong[1] National Tsing Hua University, Taiwan	**O1.3 (P1.17) Systematic study of direct laser fabrication of polymer materials on PDMS** Wang, Priscilla [1]; Goh, Zhen Ke [1]; Qi, Kaiqing [1]; Wan, Adams [1] 1. SIMTech Ltd, 2. NUSTech, A*STAR, Singapore	**O1.4 (P1.18) Temperature dependent creep characterization of lead-free solder alloys using nanoindentation** Gadsch, Stefan [1,2]; Manhart; Karlo Vollmarshof [1]; Meier; Karsten [1]; Gaitzsch; Holm [2]; Mueller; Martin [1]; Kaestner; Marcel [1]; Wolland; Marcel [1]; Beck; Gottfried [2] 1. Institute of Electronic Packaging Technology, Technische Universität Dresden, Germany; 2. Global Foundries Dresden, Germany	**O1.5 (P1.19) Flip Chip CSP Package Integrity and Reliability Evaluation** Liu, Jianwei[1] NXP, China, People's Republic of	**O1.6 (P1.20) Research on technology and mechanical aging of movable wind module sensors interconnect** Qu, Yiqu; Chen, Huanqing; Wu, Ping; Qian, Shu; Wang, Lianchang; Zhu, Weihua[1] Central South University, China, People's Republic of China	
5:20pm - 6:40pm	**O1.7 (P1.21) Assembly Process Characterization of SiO Bonding of Heterogeneous Chiplets** Lee, Sharon Mi Sung; Lee, Boon Long; Chai, Tai Chong; Ho Teng Long[1] Institute of Microelectronics, Singapore	**O1.8 (P1.22) Room Temperature Plasma-Enhanced Medium-Kiddum Wafer Bonding for 3D Integration of Superconducting Interconnects for Quantum Processing** Gale, Steven [1]; Hemanth Kumar; Chamoli; Jaswant; Hemanth Kumar [1]; Hu; Liangqing [1]; Wuen; Bienvenue [1]; Jeffery; Rachelle [1]; Huang; Ding [1]; Lau; Chi Ho [1]; Ramanujan; Ramakrishna [1]; Hongqi; Li [1]; Sun; Chuan Seng [1,2]; Chai; Ying Jian [1] 1. Institute of Microelectronics, Singapore; 2. Nanyang Technological University, Singapore; 3. Institute of Materials Research and Engineering, Singapore	**O1.9 (P1.23) Investigation of Fold-Free Chip-to-Chip Bonding Methods for CMOS-MEMS Compatibility** Tan; Y. Hsuan; Wei; Xue Jiang; Ching Chen; Daniel Guo Hao; Chang; Ser Chiang[1] Institute of Microelectronics, A*STAR Research Entities, Singapore				

DAY 3: DECEMBER 8, 2022 (FRIDAY)

Venue	Canary 1	Canary 2	Orcide	Pelican	Kingfisher	Nightingale	
08:30am -09:00am	**Invited Talk 7** New Innovation of Heterogeneous Integration in AI and ML, Eng. (Jin Yang, Samsung)	**Invited Talk 8** Fluxless Bonding for Higher Density & Bandwidth Packaging (Steve Ng, KnS)	**Invited Talk 9** Signal and Power Integrity Performance of CoWoS-R in Chiplet Integration Applications (Chuan-Tang Wang, TSMC)	**Invited Talk 10** Fan-out Wafer Level Packaging Solutions for mmWave applications (Tanya Braun, Fraunhofer IZM)	**Invited Talk 11** Modeling and Characterization of Single Grain Solder Micro Bumps in Advanced Packaging (Jeffrey Suhling, Auburn Univ.)	**Invited Talk 12** Die-to-Wafer Hybrid Bonding to Address Next-Gen Electronics Packaging Challenges (Avi Shartsman, Applied Materials)	
09:00am - 10:00am	F1. Advanced Packaging Technologies II	F2. Interconnection Technologies I	F3. Materials for Packaging	F4. Assembly and Manufacturing Technology I	F5. Mechanical Simulation & Characterization VI	F6. Materials and Processing III	
09:00am - 09:20am	**F1.1 (P1.24) Study on board-level reliability of power components on ultra-high density PCB assemblies** Su, Xiang; Shi, Hongbin; Li, Mengyuan[1] Huawei Technologies Co., Ltd., China, People's Republic of	**F2.1 (P1.25) Microstructural and mechanical analysis of Cu/Sn/Cu microbumps by doping Al and Zn into Cu substrate** Huang, Pei-Wei; Lin, Tai Wei; Dai, Jeng Gong[1] National Tsing Hua University, Taiwan	**F3.1 (P1.26) The Development of a Non-Hermetic Ceramic Package Made Flat for High-Reliability Applications** Rai, Jai [1]; Ge, Phuong [1]; Kaab, Daniel [1]; Chiang, Yaqueo [1]; Hicks, Ian [1]; Wu, Jai [1]; Hu; Vincent [1]; Zhao, Qishuo [1]; Pedro; Ric [1]; Trichur, Ramachandran [1] 1. Kemet Corporation, Irvine, CA, USA; 2. Kemet Corporation	**F4.1 (P1.27) Epoxy Mechanical System design for characterizing multiple adjacent free space optical interconnect components** Ramamoha, Shashid Kumar; Mathur; Ramana Kumar; Ra; Rajesh; Pamidighantam; Ramana; Murugesh; Rahim Samad LightQuanta Photonics Private Limited, Singapore	**F5.1 (P1.28) TIV wafer warpage simulation by multi-layer strong layer and shear-type equivalent modeling method** Ma, Xiaodong [1]; Chunhe; Ma; Shenlong[1] Lenovo university, China, People's Republic of	**F6.1 (P1.29) Characterizing Sub-micron 3D Defects From Metal Enhanced Packages to Molten Level Packaging using a Suite of Novel 3D Aux & Neural Networks Ft.5 µm Spatial Resolution** Lau, Eric; Qiao, Jeff; Dai; Shenxu; Qin, Tianxu; Jiang, Sylvia; Tan, Wenlong[1] Sigray Inc, United States of America	
09:20am - 09:40am	**F1.2 (P1.30) Development of underground structure cover with UV for radio wave transmission** Ri, Kaoshong [1]; Takeshi; Kishi [1]; Yamagata; Tatsuya [1]; Sai; Nobukiro [1]; Yamaguchi, Tatsuya [1]; Kanaya, Haruichi [1] 1. Kyocera University, Japan; 2. HIROSE Holdings Co., Ltd; 3. HIROSE, Ltd	**F2.2 (P1.31) Low temperature bonding of Cu/Sn@Ni Cu with 5µm microbump for high temperature applications** Wu, Zhi-Hao; Chen, Po-Ru; Goh, Jong Kang[1] National Tsing Hua University, Taiwan	**F3.2 (P1.32) Polymer Dielectric Layer Wetting paste for die attach application** Tan, Min [1]; Han, Xuetian [1]; Li, Hongxia [1]; Ma; Ji [1]; Chen, Fei [1]; Peyne, Dean [1]; Liu, Nan [1] 1. Indium Corporation of Suzhou, Suzhou, 215126, China; 2. Indium Corporation of Suzhou, Suzhou, 215126, China; 3. Indium Corporation, New York, 13501, USA	**F4.2 (P1.33) Package Design Characterization Advancing Substrate Metal Crack in BGA Package** Chin, Jasmine [1]; Tuan, Tu-Anh [1]; Ramanan, Sandeep [1]; Koh, Martin [1] 1. NXP Semiconductors, Malaysia; 2. NXP Semiconductors, Austin, Texas	**F5.2 (P1.34) Experimental and Numerical Investigation of Die Shift in Large Panel Level Packaging** Lum, Jing Ho; Gu, Binli ERSIntelligentmics, Singapore	**F6.2 (P1.35) Ultrafine Bump Metrology Multilayer Layer – Between for 7NM/5NM Bump Pitch at Low Thermal Budget for CZM and NCM Bonding Applications** Chamoli, Jaswant; Hemanth Kumar; Hao Jiang; Sharon Lee; Li, Hong Miao; Venkatraman, Nandini; Bhowmik, Chandan; Rao; Chai, Ying Jian; Vempati, Srinivasa Rao; Singh, Navneet Institute of Microelectronics, A*STAR, Singapore	
09:40am - 10:00am	**F1.3 (P1.36) Influence of Parasitic Power Loop Inductance on Switch Performance in GaN HEMT** Ma; Ping Ma; Chuanqian; Qu; Yiqu; Qian; Shu; Wang; Lianchang; Zhu; Weihua[1] Central South University, China, People's Republic of China	**F2.3 (P1.37) Analysis on bending wires of Au-Coated Ag alloy for BGA automotive application** Palagiad; Jose; Lim; Teck Gang; Sutaman; Jasmine; Nur Darwisyah; Mazlan; Fitri; Koh Inn; Wang; Soon Wei; Ghazali; Omar On Semi, Malaysia	**F3.3 (P1.38) Low Super Power Path Bonding for RF Voltage Drop Reduction in Automotive Sets** Sharma, Ajay Kumar; Kumar; Jaswinder; Bhandari, Rishi; Jain, Sanjayan[1] NXP Semiconductors pvt ltd, India	**F4.3 (P1.39) uPoP: Innovation Solution for Mobile Memory Package** Li, Brian; Sun, Isaac; Shi; Stephen; Zhu, James; Fan; Tao; Quan, Changhao; Wei, Charles[1] Changxin memory technical, China, People's Republic of	**F5.3 (P1.40) Virtual Design of Experiment Methodology for Package Design Robustness** Gaya, Navneet[1] ERSIntelmetrics, Malta	**F6.3 (P1.41) Realizing ultra-thin high-reliability storage devices with large capacity by package and PCB collaborative design** Wu, Hongbin; Yang, Chao; Zhang, Jianxu[1] Huawei Technologies Co., Ltd	
10:00am - 10:20am	Coffee/Tea Break (Grand Ballroom Foyer)						
10:20am - 11:50am	Canary 1	Canary 2	Orcide	Pelican	Kingfisher	Nightingale	
	G1. Thermal Management II	G2. Interconnection Technologies II	G3. Materials and Processing IV	G4. Assembly and Manufacturing Technology II	G5. Failure Analysis II	G6. TSV/Wafer Level Packaging	
10:20am - 10:50am	**G1.1 (P1.42) 1 High flow rate piezoelectric micropump for miniature liquid cooling systems** Kao; Shawn; Zhang; Kinfeng; Ang; Guanying; Kang; Jinqi; Hu; Ruo; Jiao; Kunbing[1] Nanyang University of Science and Technology, China, People's Republic of	**G2.1 (P1.43) Eliminating Preferred orientation and Parting Grain Size with Stepping in Electro-Plated Cu Pillars for Improving under-bump metallurgy Assessment** Chen, Chen-Sung; Chen, Zi-Xu; Duh, Jenq Gong[1] National Tsing Hua University, Taiwan	**G3.1 (P1.44) Dry Film Resin with Four Key Technologies to Achieve 1/S=1/1 µm Patterns** Higgoshi, Kei; Tada; Nobuaki; Yoshikawa; Kensuke; Kaguchi; Yusuke; Funai; Kensaku; Kawada; Hideaki; Iwanchi; Kenichi[1] Resonac Corporation, Japan	**G4.1 (P1.45) Integration of plasma dicing in the collective die to wafer hybrid bonding** Sabaut; Samuel [1]; Kamen; Rami [1]; Bos; Pieter [1]; Stoecker; Fritz [1]; Worley; Edward [1]; Bauer; Gerald [1]; Bauer; Gerald [1]; Bayne; Kris [1,2] 1. ASMC, Belgium; 2. ASL, UK	**G5.1 (P1.46) A Novel Burn Out Failure of Microbump During Electromigration** Lee, Yikun [1]; Ho; Yuanxun [1]; Fu; Kang Ming [1,2]; Liu; Yongxia [2] 1. Department of Materials Science and Engineering, City University of Hong Kong, Hong Kong S.A.R. (China); 2. Department of Systems Engineering, City University of Hong Kong, Hong Kong S.A.R. (China); 3. Department of Electrical Engineering, City University of Hong Kong, Hong Kong S.A.R. (China)	**G6.1 (P1.48) Demonstration and Challenges of Through Elastomer (TE) with Super Resilable Cu-nanotwinned Super Bumbable Cu Bits** Tang, Ye Ching; Chai, King Jien[1] Institute of Microelectronics Agency for Science, Technology and Research (A*STAR), Singapore	
10:50am - 11:10am	**G1.2 (P1.52) Development of a novel flow-assisted liquid cooling of 3D ICs via 3D printing** Hong; Huichang; Tang; Dongsun; Zhang; Xiaoxu; Lee; Boon Long; Jang; Ming; Chou; Ai Ling; Ho; Soon Wee; Lim; Sheng; Ser Hui; Ong; Kim Leon; Li; Hongqing; Ho; Siew Lok; Jing[1] A*STAR, Singapore	**G2.2 (P1.51) Laser Direct Structuring (LDS) for enhanced QFN package** Catalano, Giancarlo; Cecchetto; Luca; Sanna; Jacopo; Verardi; Jessica; Villa; Riccardo; Vitello; Gianluli ETMIntelmetrics, Italy	**G3.2 (P1.53) Process development, characterization and electronic evaluation of green laser induced graphene from polyimide** Liu; Shibo [1]; Qi; Xiaoqing [2]; Chew; Ai Ling [1]; Ho; Soon Wee [1]; Cheng; Xin Wei [1]; Ng; Siew Lok [1] 1. Advanced Manufacturing and Technology Center / Agency for Science, Technology and Research (A*STAR), Singapore; 2. Singapore Institute of Manufacturing Technology / Agency for Science, Technology and Research, Singapore (A*STAR)	**G4.2 (P1.54) Cu and barrier CMP process development for Hybrid Bond Cu pad and 2.5 µm pitch for Wafer-to-wafer 3D** Chakl Roy; Sangita; Elm Guan; Chen; Venkatraman; Nandini; Lee; Wen; Singh; Navneet Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore, Singapore	**G5.2 (P1.55) Failure Mode Evaluation of QFP Package Interconnect Structure under Random Vibration** Shimamura, Kazunori[1] Yokohama National University, Japan	**G6.2 (P1.57) Through glass vias fabrication using electro-machining and electrolysis deposition** Mazer, Karsten; Pandey; Harish; Ekeli; Prashanth Indian Institute of Technology Bombay, India	Interactive Presentations 2
11:10am - 11:30am	**G1.3 (P1.56) Design of liquid cooling unit plate for 3D IC integration based on Tesla valve and fin-shape hybrid structure** Ho; Rui [1]; Sahu; Jaydeep [2]; Tang; Dongsun [1]; Penda; Sanjib Kumar [2] 1. Institute of Microelectronics (IME), Agency for Science, Technology & Research (A*STAR), Singapore; 2. Department of Electrical & Computer Engineering (ECE), National University of Singapore (NUS)	**G2.3 (P1.61) Fine Pitch Integration (≤5 µm) Cu Pillars Bump Pitch to Wafer assembly using Hybrid Bonding** Dubey; Vikas; Wolmuth; Dirk; Grabhorst; Ricardo; Wenzel; Markus Fraunhofer IZM, Germany	**G3.3 (P1.62) Development of 3D Durable Thin Film Protection Film – W Shield Layer Power Devices** Yamachika; Shigeyuki; Kobashi; Akiyo; Sato; Saki[1] Intec Corporation, Japan	**G4.3 (P1.63) Effect of Solder Line Metal Thickness on Cu Pillar Bump Chipping for Short Power Devices** Gambino, Jeff [1]; Barbosa; Ronald [2] 1. Onsemi, United States of America; 2. Onsemi, PHILippines	**G5.3 (P1.64) Lock-in Thermography judgement of failure mode of high temperature defects in advanced Fan-Out packages** Liu; Yu Fang[1] Advanced Semiconductor Engineering, Taiwan	**G6.3 (P1.65) 3D Modeling of the Through TGV Size and Fabrication of SiC based Interposer Wafer** Mechanski, Piotr [1]; Klumpp; Julia Marie [1]; Schiffer; Michael [1]; Schneider-Ramelow; Martin [1] 1. Fraunhofer IZM, Germany; 2. Technische Universität Berlin, Germany	
11:30am - 11:50am	**G1.4 (P1.67) Innovative thermal performance evaluation of the power module structure under real operating conditions** Saito; Tomoya [1]; Hirosaka; Daisuke [1]; Ito; Gang [1]; Liu; Wei [1]; Matsuoka; Mitsutoshi [2]; Ramotsu; Yuji [2] 1. Yokohama National University, Japan; 2. Hitachi Ltd., Japan	**G2.4 (P1.67) A Conceptional Study towards Developing a Novel Copper Top Side Interconnection in Power Electronics using Additive Manufacturing** Eckel; Alexander; Kuppel; Marcel; Franke; Wolfgang Friedrich-Alexander-University Erlangen-Nuremberg, Germany	**G3.4 (Invited Talk) Die to Wafer (D2W) Polymer Bonding for Advanced Heterogeneous Integration** Jonathan Abbitt BESI	**G4.4 (P1.68) Compensation Analysis of Laser Parameters effect on Laser Splash Performance in UV/Vis/I Sheath Dicing Tools** Ganesh; Nathanael Simon; Harish Shah; Ankur; Sunita; Bennett Liu; Jenny Sim; Chris Singh; Harry[1] Micron Semiconductor Asia Pte Ltd, Singapore	**G5.4 (P1.71) A Board-Level Vibration Test Method for Electronic Industry Application** Lee; Jeffrey Chengfeng [1]; Ho; Yongi [2]; Hsieh; Hsiao; Jeffery [2] 1. ST Integrated Service Technology Inc., Taiwan; 2. Nexlite Corporation, 5. ASDRAS, Inc.	**G6.4 (P1.72) Evolution of Nano-notches on the Surface of SiC with Different Crystal Forms during Cutting in the Water Environment** Chen; Yuqi; Lu; Wenhuan; Zhu; Fulong[1] Nanchang University of science and technology, China, People's Republic of	
Venue	Ballroom A + Ballroom B		Grand Ballroom foyer				
11:50am - 1:20pm	**Young Professionals' Event** (12:20pm - 1:20 pm)		Buffet lunch in foyer				
Venue	Ballroom A + Ballroom B		Orcide	Pelican	Kingfisher		
1:20pm -2:40pm	**HIR workshop**		H3. Materials and Processing V	H4. Electrical Simulations & Characterization I	H5. Packaging Technologies & Solutions II		
1:20pm - 1:40pm			**H3.1 (P1.73) Guard Cut TM Applications to Eliminate Dicing Edge Chip out** Mazer; John Chasen; Gray; William; Ignacio; Francisco[1] Dantec LLC, United States of America	**H4.1 (P1.74) Time-interval Error (TIE) based Design and Characterization of DDR5 Data Strobe Signaling** Park; Shimpung [1]; Arjun Haldar; Vinod [1]; Ji 1. Rambus Inc., United States of America; 2. Rambus Inc., India	**H5.1 (P1.75) Qualification of High Capacity Large Package for Advanced Computing and Gaming** Murthy; Ratna [1]; Kanaran; Sreedharan Kalappan [1]; Ramachandran; Premkumar [1]; Michael; Bernard Raj [1]; Gunasekaran; Jayaprakash [1]; Ahmed; Ashraf [1]; Karuvalbaram; Rajgokhan [1]; Sulaiman; Muhammad Afiq [1] 1. Fiec 2. ASEE	
	1:20pm - 1:25 pm Welcome & Agenda Review by William Chen and Mahajan 1:25 pm - 2:00 pm Keynote Address by Chuan Khoon Lim, Senior VP, ASM Pacific						
1:40pm - 2:00pm			**H3.2 (P1.76) High Precision Wafer Thinning Using Glass for TPV Glass Carrier and Novel Temporary Bonding** Zhang; Leyli Corning Incorporated, United States of America	**H4.2 (P1.77) Simulation study of the influence of Power Integrity on the high frequency planar inductor in DC-device application** Maeoka; Seiya; Ohno; Akihiko; Miyata; Masato; Sasaki; Hiroyuki; Takahashi; Hideaki[1] FUJITSU Corporation, Japan	**H5.2 (P1.78) Simulation study of the influence of Power Integrity on the high frequency planar inductor in DC-device application** Maeoka; Seiya; Ohno; Akihiko; Miyata; Masato; Sasaki; Hiroyuki; Takahashi; Hideaki[1] FUJITSU Corporation, Japan	
2:00pm - 2:20pm	2:00 pm - 2:10 pm HIR Briefing by William Chen 2:10 pm – 2:20 pm 20-SD & interconnect by Ravi Mahajan		**H3.3 (P1.1) Investigation of Innovative Dielectric Materials and Processing Methods Made for Flat Optics with Aperture on Chips** Tang, Chin Sheng; Tobing; Landobasa Y. M.; Ho; Jun Chi; Singh; Navneet[1] A*STAR - Institute of Microelectronics (IME), Singapore	**H4.3 (P1.2) Design of Four-Way Multiplexer using Lumped Elements for Qubit Characterization** Ravanugam Bhaskar; Vignesh; Dragos; Roberu; Mihai[1] Agency for Science, Technology and Research, Singapore	**H5.3 (P1.3) Assembly of Thin Silicon Chiplets using Laser-Induced Forward Transfer** Kamoyia; Kariuki; Kumar [1,2]; Van Hoenbergs; Geert [1,2] 1. Center for Microsystems Technology (CMST), IMEC, Belgium; 2. Ghent University, Belgium	
2:20pm - 2:40pm	2:20 pm - 2:30 pm Mobile by Raman Chan 2:30 pm - 2:40 pm Modelling & Simulation by Chris Bailey		**H3.4 (P1.5) Various dicing approaches for Silicon Carbide Wafers** Jeon; Yuju Ko; Seokho; Kim; Minkoo; Bae; Jaehyun Ryu; Dongho; Park; Dongjun; Park; Kyunghee[1] Amkor Technology, Korea, Republic of (South Korea)	**H4.4 (P1.7) Fine-tuning of piezoresistive sensors (PRS) in Microfluidic Lab-on-a-chip (LoC) for Cell Mechanotyping** Tschudin; Christian[1] Fraunhofer IZM, Germany	**H5.4 (P1.8) Effect of adhesive behavior and mechanical properties on the delamination of photolithography Microstructure structure** Li; Jiang; Yuji Kanazawa Polytechnical University, Ishikawa, People's Republic of China	
2:40pm - 3:00pm	Coffee/Tea Break (Grand Ballroom Foyer)						
3:00pm - 4:20pm	**HIR workshop (continued)**		I3. Materials and Processing VI	I4. Packaging Technologies & Solutions III			
3:00pm - 3:20pm	3:00 pm - 3:10 pm Co-Design by Jose Schutt-Aine 3:10 pm - 3:20 pm Supply Chain by Kitty Pearcall		**I3.1 (P1.9) Characterization and Analysis of High Efficiency in Aqueous-Based Flux Cleaning Process for High Voltage Power Device Packages** Ramalingam; Nagarasuriya; Manuka; Jeewanda Samaraweli Renesas Malaysia Sdn Bhd	**I4.1 (P1.11) Assessment of Delamination Risk During Sawing Process by Simulation** Tatsuya; Kharisa Sihuan; Kang; Chen Wei; Hong; Kim			
3:20pm - 3:40pm	3:20 pm - 3:30 pm Integrated Power Electronics by Patrick McCluskey 3:30 pm - 3:40 pm SiP & Module by Erik Jung		**I3.2 (P1.12) In-Package Relative Humidity Sensors with Multi-Functional Capabilities Towards Advanced Reliability Characterization of Packaging Encapsulation Materials** Sabari; Ramnac; van Zeijl; Henk; Zhang; Guoqi[1] Delft university of technology, Netherlands	**I4.2 (P1.13) Adhesive Fracture Analysis of Die Attach Film Laminated Tape by Peel Test** Chen; Fachang; Yang; Kai; Cheng; Yu Sang[1] Infineon Technologies Asia Pacific Pte Ltd, Singapore			
3:40pm - 4:00pm	3:40 pm - 3:50 pm Test by Haiker Zhang 3:50 pm - 4:00 pm HIR Workshop Wrap Up by William Chen & Ravi Mahajan		**I3.3 (P1.14) The path to several method for the orientation information attribute in composites** Zhang; Kinfeng; Ren; Shuan; Yang; Guan; Ang; Jinqi; Ang; Guanying; Hu; Ruo; Jiao; Kunbing[1] State Key Laboratory of Combustion, School of Energy and Power Engineering, Nanchang University of Science and Technology, Wuhan 430074, China	**I4.3 (P1.15) Comp of piezoresistive dataset (PRS) in Microfluidic Lab-on-a-chip (LoC) for Cell Mechanotyping** Ou; Yanxiang; Jun; Sungsik; Jeon; Jongkyung; Kim; Minjung Samsung; Korea			
4:00pm - 4:20pm			**I3.4 (P1.16) Wire loop characterization for wire sweep evaluation** Jeanne; Federico; Caglio; Caroline; Vincent; Fabien; Olivia; Riccardo ETMIntelmetrics, Italy				
4:20pm - 5:00pm	Grand Ballroom Foyer						
	Closing Ceremony and Lucky Draw						